

Christopher Brian Walton

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Objective:

R&D position focused on the performance and architecture of new computer systems and networks.

Research and Development Experience:

Senior Software Developer, HyPerformix, Inc., Austin, TX, 5/2005 to 5/2010 Lead developer for the analytic modeling engine in *HyPerformix IPS Capacity Manager™*, a state of the art enterprise capacity planning program.

- Worked with chief scientist to extend standard Queuing Network Model (QNM) techniques to handle server consolidation and virtualization. Coauthored patent application for this work.
- Refined techniques to generate QNM of enterprise computing systems from measured performance data.
- Coded and tested modeling algorithms in VB.NET and C#.NET.
- Refactored monolithic modeling engine code using Ninject dependency injection framework.
- Developed an approach to write a formal specification of QNM in Mathematica that generates an executable model. Output of this model is used to verify the modeling engine in the product.
- Advised consultants, technical support and customers on model design and validation.
- Defined test cases with predicted numerical results.
- Resolved product defects and performed general pre-release QA tasks.

Senior Quality Assurance Engineer, TippingPoint Technologies, Austin, TX, 9/2003 to 4/2005.

- Tested intrusion prevention systems, security management systems, and attack filter sets for performance, functionality, accuracy and robustness.
- Developed new test cases, especially accuracy and stress tests for traffic shaping capabilities.
- Wrote scripts in TCL/Expect and Perl for software installation, test automation, and data reduction.
- Planned, budgeted, and implemented new QA lab, including hardware installation, designing the lab network, OS installation and setting up DNS, NFS, and Samba servers.

Independent Consultant, 1/2002 to 9/2003.

- Simulation modeling of HyperTransport protocol for Flow Engines, a storage network startup.
- Benchmarked Java-based XML parsers for Conformative Systems, an XML acceleration startup. Used design of experiments and analysis of variance to isolate the effects of platform, workload and application implementation on performance.

Principal Performance Scientist, Sariga Networks, Austin, TX, 3/2001 to 12/2001. I was key member of a start-up team developing innovative technology for packet voice systems and chips. Contributions included:

- Helped develop a new real-time scheduling algorithm with arbitrary constraints on scheduling delay.
- Proved mathematically that a new scheduling algorithm provided optimal jitter reduction within delay constraints.
- Wrote and validated detailed simulation of scheduling algorithm.
- Wrote simulation of complete scheduling architecture, including voice and data sources, DWRR and WRR schedulers, and token bucket rate control.

Member of Technical Staff, Agere Systems/Lucent Microelectronics, Austin, TX, 1/2000 to 2/2001. I helped guide the design of a 10Gbit/sec network processor chipset (packet classifier and traffic manager) on a daily basis. My contributions included:

- Developed a detailed Queuing Network Model (QNM) of 10G classifier, written in Mathematica. This was the only way the team could evaluate performance until a simulation came on line late in the development cycle. Analytic throughput predictions were within 10% of detailed simulation result.
- Extended standard QNM techniques to model pipelined and replicated service centers
- Wrote wrapper code for QNM model to automatically tune load to reach a target utilization of bottleneck resource.
- Simulation study of buffer management for 10G Traffic Manager.
- Characterized network workloads for use as input to both analytic and simulation model.
- Generated test programs and test data sets for simulation.
- Supported simulation validation by experimental design and results analysis.

Systems and Software Engineer, Telecommunications Platform Division, Compaq Computers, Austin TX, 3/1994 to 12/1999. As a senior analyst, I used my skills in modeling, benchmarking, and analysis to improve the performance of hardware, system software and middleware for fault tolerant UNIX platforms. Accomplishments include:

Performance Modeling:

- Developed analytical performance model to compare performance of several APIs for remote DMA.
- Analytically modeled a large customer cellular telephony application, revealing that initial design would not meet its performance requirements.
- Wrote simulation model of the same project to provide detailed information about performance characteristics months before measurements were available.
- Sized many large, complex customer applications, often working directly with customer's technical staff.
- Debugged and enhanced an advanced Markov chain availability model for clustered UNIX systems, then recommended changes to improve availability.
- Used mean value analysis (MVA) to model lock acquisition delays.

Performance Measurement and Analysis:

- Benchmarked and analyzed performance of TCP/IP over Ethernet and ATM.
- Benchmarked and analyzed SS7 performance.
- Ensured that performance requirements in contracts for custom products were both realistic and unambiguous.
- Advised customers on how to write efficient applications.
- Instrumented code for TCP/IP and network device drivers.
- Used advanced statistical methods to organize parameter tuning experiments for TCP/IP software.
- Served on team that made 20X thrupt improvement in new Ethernet controller.

Tool Development:

- Developed a script-driven tool to measure TCP/IP performance. The tool automatically scales workloads and collects statistically valid latency, thrupt and CPU utilization data.
- Used Flex/Bison to implement command language for TCP/IP performance tool.

Quality & Other:

- Wrote procedures and checklists for performance reports, investigation of customer performance complaints, and error analysis.
- Served on assessment team for SEI CMM level 3.
- Trained and experienced software inspector, using Fagan method.
- Interviewed job candidates at all levels

Advisory Programmer, IBM LAN Systems, Austin, TX, 4/1992 to 2/1994. Identified, quantified, and advocated performance improvements in Multi-Protocol Transport Services for OS/2 (MPTS). Provided daily guidance and training to second analyst assigned to MPTS, and acted as consultant to others working on OS/2 transport performance. Specific accomplishments included:

- Developed analytic model of multimedia servers on Ethernet.
- Designed simulation of gateway buffer manager.
- Tracked performance of OS/2 transports.
- Integrated performance trace hooks into production code for transport drivers.
- Used traces to measure time spent in each protocol layer.
- Measured checksum overhead in TCP/IP.
- By tracing buffer usage during a variety of scenarios, formulated recommendations for start-up buffer allocations.
- Measured working sets of transport device drivers.
- Advised developers on performance implications of design choices, keeping some severe bottlenecks out of design.

Development Staff Member, Austin Programming Center, IBM-Austin, 9/1991 to 3/1992.

- Developed analytic model of OS/2 database manager utilities.
- Prototyped and measured performance improvements.
- Measured working set of OS/2 Database manager

Research Scientist Assistant, UT-Austin, 7/1988 to 8/1991.

- Developed taxonomy and performance model of data skew in parallel joins.
- Used analytic and simulation modeling to analyze effects of data skew on database machine performance.
- Wrote technical reports and conference papers.
- Measured skew in existing databases.
- Participated in writing grant proposals

Digital Computing Analyst, United Technologies Research Center, East Hartford, CT, 7/1981 to 8/1984.

- Programmed FORTRAN applications for data reduction, graphics, and simulation.
- Wrote assembler code to interface lab equipment to PDP-11 minicomputers.
- Modified source code and provided object code patches to support testing of a microprocessor-based controller for automotive diesel engines.
- Analyzed hardware and software requirements for new or modified data acquisition systems

Education

Ph.D. (Computer Sciences), University of Texas at Austin, 5/1992

Dissertation: *Skew and Scalability of Parallel Joins on Multicomputers*

GPA: 3.67/4.00

M.S. (Computer Science), Worcester (MA) Polytechnic Institute, 10/1986

Thesis: *Implementation of IEEE Standard 802.2 on an Ethernet Local Network*

GPA: 4.00/4.00

B.S. (Physics), *magna cum laude*, Bates College, Lewiston, ME, 6/1981

Thesis: *A Carbon Dioxide Laser: Construction and Basic Theory*

GPA: 3.71/4.00 overall; 3.83/4.00 in major

Systems and Language Experience

Simulation Software: OpNet, SES/Workbench, Csim, GASP

Programming Languages: C#, Visual Basic, Perl, Mathematica, TCL/Expect, Java, FORTRAN, PASCAL, MODULA-2, LISP, BASIC

Assembler Languages: VAX, PDP-11, Intel x86, Z80, 6502, IBM 360/370

Operating Systems: UNIX (SVR4, UnixWare, SunOS, Linux);
Windows NT/2000/XP; OS/2; Mac OS, VAX/VMS, RT-11

Patent:

Method and Apparatus for Using Multiple Reassembly Memories for Performing Multiple Functions, with G.A. Bouchard, M. Calle, J.R. Davidson, M.W. Hathaway and J.T Kirk, assigned to Agere Systems, Inc. Patent granted in European Union, application pending in U.S. and Taiwan.

Publications

- *Partition Data Skew and the Scalability of Parallel Joins*, Symposium on Parallel and Distributed Processing, Dallas, 12/91
- *A Taxonomy and Performance Model of Data Skew Effects in Parallel Joins*, Very Large Database Conference, Barcelona, 9/91 (with A.G. Dale and R.M. Jenevein)
- *Measurement of Data Skew in Two Databases*, UT-Austin Computer Sciences Dept. Technical Report TR-90-32, 9/90 (with M. Pinsonneault and F. Haddix)
- *Four Types of Skew and their Impact on Parallel Join Performance*, UT-Austin Computer Science Dept. Technical Report TR-90-12, 5/90
- *Scalability of Parallel Joins on High Performance Multicomputers*, UT-Austin Computer Sciences Dept. Technical Report TR-89-39, 12/89. (with A.G. Dale, F. Haddix, and R.M. Jenevein)
- *A Laboratory for Local Area Network Measurement Experimentation*, 11th IEEE Conference on Local Computer Networks, Minneapolis, 10/86 (with R. Kinicki and P. Chiang)

Graduate Coursework:

Operating Systems, Networks, Real-Time Systems, Simulation, Systems Performance, Distributed Computing, Parallel Programming, Database Management, Database Implementation, Database Machines, Graphics, Compilers, Software Engineering, Artificial Intelligence

Teaching Experience:

Guest Lecturer on "Performance Analysis through the Software Lifecycle" for undergraduate software engineering class (CS 373 at UT-Austin) from Fall 1997 to Fall 1999. Also acted as mentor for teams of students working on term projects.

Teaching Assistant, UT-Austin, 9/87 to 6/88. Taught recitation sections, wrote and graded assignments and exams

Reviewed textbook manuscripts for Little-Brown, 1985 and 1986.

Instructor, Worcester Polytechnic Institute, summer 1985. Responsible for teaching and administration of a sophomore course in assembly language programming and computer architecture. Wrote a complete set of lectures and assignments in response to the installation of a new computer system. Many of the materials were subsequently included in a new textbook.

Teaching Assistant, Worcester Polytechnic Institute, 9/84 to 6/86. Taught recitation sections, supervised labs, graded programs and reports.

Honors, Grants, and Awards

- Elected Senior Member of IEEE, August 2002
- Received NSF (National Science Foundation) grant for intensive Japanese language study (at Middlebury College), summer 1990
- MCD (Microelectronic and Computer Development) fellowship, UT Austin Department of Computer Sciences, 1986-87 academic year.
- Upsilon Pi Epsilon, Worcester Polytechnic Institute, 1985-86 academic year
- Presidential Scholar Award, Worcester Polytechnic Institute, 1984-85 academic year
- Phi Beta Kappa, Bates College (Gamma of Maine chapter), 1981

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References Available upon Request.